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EXAMINER	
LE, BRIAN Q	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/828,003	Applicant(s) SUZUKI, EIKO
	Examiner Brian Q Le	Art Unit 2623

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-12 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-12 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 06 April 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4-5.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 5-8 and 12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Regarding claims 5, the Examiner finds that the specification does disclose the image sensing optical means which executes retry processing of performing ID recognition in according **with first and second read optical** (emphasis added) conditions integration. Further details are needed to clarify these claim limitations. Regarding claim 12, the Applicant also does not clearly disclose in the specification referring to a wafer's ID recognition process wherein the ID includes the combination of first ID and second ID from code information and character/numeral information. Furthermore, the Applicant needs to point out where (page and line number) a recognition processing means perform digital recognition processing of the first ID and perform analog recognition on the second ID if no code can be recognized. The Examiner asserts that the Applicant discloses a concept of digital recognition and analog limitation. However, the Applicant does not disclose the claimed limitation. Claims not specifically addressed depend from indefinite antecedent claims.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 5, 8-9, and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Ono Satoru JP10-227184.

Regarding to claim 1, Ono teaches a semiconductor wafer ID recognition apparatus (Detailed Description, first paragraph) comprising:

Image sensing optical means for reading at least one identification information (ID) marked at an arbitrary position on a semiconductor wafer in accordance with a plurality of first read optical conditions registered in advance (Detailed Description, first paragraph); and

Recognition processing means for performing recognition processing (Detailed Description, page 1, last paragraph) including calculation of an evaluation score representing a read likelihood ratio for an image output from said image sensing optical means every read optical condition (Detailed Description, page 3, second paragraph and Table 1), and adopting a recognition result under a read optical condition exhibiting the highest score ("optimum value based on the recognition result") as an ID of the semiconductor wafer (Detailed Description, page 4, first 20 lines).

For claim 2, Ono further teaches an apparatus wherein said recognition processing means performs recognition processing for a corresponding ID among a plurality of IDs recorded on the

semiconductor wafer in accordance with the first read optical conditions, and adopts, as the ID of the semiconductor wafer, a recognition result under a read optical condition exhibiting the highest score obtained by recognition processing under all the first read optical conditions (It is the process of calculating the highest score under optical reading conditions) (Detailed Description, page 4, first 20 lines).

Referring to claim 5, please refer back to claim 1 for the explanation.

For claim 8, Ono teaches an apparatus wherein said recognition processing means determines that no ID can be recognized when an evaluation score is under a predetermined value or when an indistinct character exists in a character string of a recognition result (Detailed Description, page 3, second paragraph, table 1, and page 4).

Referring to claim 9, please refer back to claim 1 for previous claimed limitation. In addition, Ono teaches a light source which is arranged to irradiate an ID on the semiconductor wafer and changes in irradiation condition in accordance with the first read optical conditions, and image sensing means for reading the ID on the semiconductor wafer irradiated by said light source (Solution and Means, page 1), and said recognition processing means comprises read optical condition memory means for storing the first read optical conditions, light source control means for controlling said light source so as to set the first read optical conditions stored in said read optical condition memory means (Camera has memory to store the optical conditions) (Solution).

Regarding claim 11, Ono discloses an apparatus further comprising transfer means for transferring the semiconductor wafer to a predetermined position on the basis of the ID adopted by said recognition processing means (Detailed Description, page 2, last 15 lines).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3, 6-7, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Ono Satoru JP10-227184 and Hunter U.S. Patent No. 6,697,517 as applied to claim 1 above.

Regarding claim 3, Ono does not clearly teach the apparatus further comprising informing means for generating a warning when no ID can be recognized by recognition processing under the first read optical conditions. Hunter teaches a process of recognizing substrate/wafer that further verify the signature/ID on each substrate through video image and that each signature is verified to ensured if each substrate is by passed (column 13, lines 8-41). Thus, it would have been obvious that there is a warning message shows on the video image system to give warning if the signature on a substrate/wafer is not correct. Modifying Ono's method of wafer's ID recognition according to Hunter would able to further help the system to generate warnings if the ID is not correct so that the operator can further correct the wafer's ID. This would improve processing and therefore, it would have been obvious to one of the ordinary skill in the art to modify Ono according to Hunter.

Regarding claims 6-7, please refer back to claim 3 for further explanation.

Regarding claim 10, please refer back to claim 1 for further explanation. However, Ono does not explicitly teaches a memory (a computer system) to store the recognition result said recognition unit and an evaluation result of said evaluation unit. However, Hunter teaches a computer system with memory is used to generate software and store information for the process of recognizing substrate/wafer's ID. Modifying Ono's method of wafer's ID recognition according to Hunter would able to further help the system providing memory for storing the recognition result and evaluation result of said evaluation unit. This would improve processing and therefore, it would have been obvious to one of the ordinary skill in the art to modify Ono according to Hunter.

CONCLUSION

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to semiconductor wafer ID recognition concepts:

U.S. Pat. No. 6,236,903 to Kim, teaches Multiple reaction chamber system having recognition system and method for processing wafer.

U.S. Pat. No. 5,909,276 to Kinney, teaches optical inspection module and method for detecting particles and detects on substrates in integrated process tools.

U.S. Pat. No. 6,707,544 to Hunter, teaches particle detection and embedded vision system to enhance substrate yield and throughput.

U.S. Pat. No. 4,499,595 to Masaitis, teaches system and method for pattern recognition.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Q Le whose telephone number is 703-305-5083. The examiner can normally be reached on 8:30 A.M - 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amelia Au can be reached on 703-308-6604. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306 for regular communications and 703-872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC Customer Service whose telephone number is 703-306-0377.

BL
May 11, 2004

SAMIR AHMED
PRIMARY EXAMINER